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High Efficiency Buck Converter for Electronic Devices in CMOS Technology

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Abstract—*This paper presents design of a high efficiency buck converter using off-chip L & C circuit and a compensation circuit. The circuit works on discontinuous current mode. The proposed buck converter improves efficiency up to 90% by switching at a switching frequency of 1 MHz between supply source and storage circuit for a voltage conversion from 3.3 V to 1.5 V giving maximum current of 500 milli amperes. By varying the duty cycle of the system, average output is controlled and this duty cycle is independent of inductor L. A feedback circuit is used for the switching purpose. But a feedback circuit has instability issues if it follows Barkhausen criteria. For a good feedback system, phase margin should be approximately equal to 60 degrees to be stable. A buck regulator shows double pole response at its peak. A double pole system has a sudden 180 degrees phase shift which makes phase margin approximately equal to 0 degree making the circuit unstable. To overcome this, a compensation circuit is needed which cancels out one pole giving a phase margin of 54 degrees. The proposed circuit is implemented in 350nm TSMC standard technology.*

1. INTRODUCTION

The growing trend of portable electronic systems like laptop, calculator, smart phones, etc shows that the need of low power devices have become very important in today's world and hence, to reduce the power dissipation is the important key to satisfy the power budget of various circuits and therefore their efficiencies. DC/DC converters form the backbone of different portable electronic devices as they supply different voltage levels in several sub-circuits of the device from a single battery supply.

The simplest way of reducing voltage level of DC supply is to use a linear regulator but it wastes a lot of energy by dissipating excess power as heat without any current step up. Switching regulators are used instead of linear regulators for achieving higher efficiency, dissipating no power ideally. Buck converter, a type of switching regulator, is a voltage step down and current step up converter. It has a remarkable efficiency, higher than 90%. [1]

Efficiency is a good measure of converter performance. A goal of current converter technology is to design converters of small size and weight which process significant power at high efficiency. High efficiency leads to low power loss within the converter. [2]

Section II describes basic working of a buck converter. Section III discusses the double pole response behavior of buck converter using its transfer function and bode plot. In the consecutive sections, the proposed circuit and its components along with simulation results and efficiency calculation are discussed in detail.

2. BUCK CONVERTER

Buck converter is a type of switched mode power supply that delivers DC output voltage at a lower level than the input voltage. It is a lossless converter which means it conserves power. Power conservation can be expressed as:

$$P_{conv} = I * V,$$

this means whenever there is a decrease in voltage (V) there will be simultaneous increase in the current (I) keeping the power conserved. The storing elements inductor and capacitor helps in this power conservation. Hence, buck converter is a voltage step down and current step up converter.

2.1. Working principle [3]

Fig. 1 shows a simple buck converter with two switches 1 & 2 controlled by a switch controller.

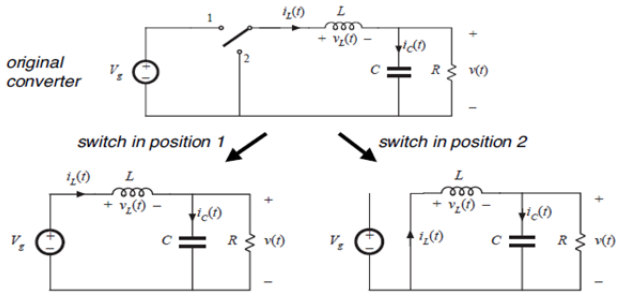

Fig. 1: Buck converter.

2.1.1. Switch in position 1. When switch 1 is on, DC source supplies voltage to the circuit and inductor stores energy by this time.

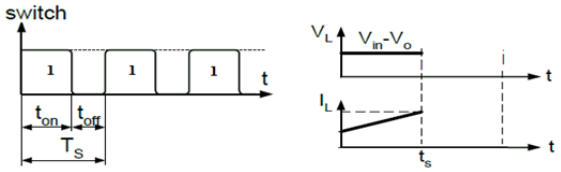

Fig. 2: Inductor voltage & current in position 1.

2.1.2. Switch in position 2. When switch 2 is on, the energy stored in inductor supplies voltage to the circuit.

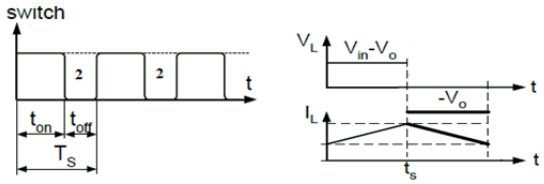

Fig. 3: Inductor voltage & current in position 2.

2.2. Duty cycle calculation

Duty cycle (D) is an important parameter that decides the duration of both the switches. The variation in t_{on}/T_s controls the average output. Section 2.1 shows the path and waveforms in both cases. Using these cases, duty cycle of buck converter is calculated.

The voltage equation of an inductor L is given by:

$$L * (di/dt) = dV \quad - \quad ----1$$

$$Or \quad di = (1/L) * dV * dt \quad -- \quad ---2$$

If we assume our converter to be in steady-state, then inductor current would be same at the start and end of period. And from Fig. 3 we can calculate inductor current as follows:

$$During\ t_{on} : di = (1/L) * V_{in} - V_o * t_{on} \quad -- \quad ---3$$

$$During\ t_{off} : di = (1/L) * V_o * t_{off} \quad - \quad ----4$$

On solving equations 3 and 4:

$$V_o/V_{in} = t_{on}/T_s = D \quad ----5$$

This is an important result as the inductor L size doesn't affect duty cycle.

3. TRANSFER FUNCTION AND BODE PLOT

Transfer function is an equation that gives relation between input and output of a system whereas bode plot gives its corresponding log-plot. These two are measures of gain response of a system. The double pole response of a buck converter can be seen from its transfer function and corresponding bode plot. And a study of its bode plot calculates the required phase margin and gain margin.

Transfer function of buck converter is given as [2]:

$$G_{vd}(s) = G_{d0} \frac{\left(1 - \frac{s}{\omega_z}\right)}{\left(1 + \frac{s}{Q\omega_0} + \left(\frac{s}{\omega_0}\right)^2\right)} \quad -- \quad --6$$

This clearly shows that buck converter has two identical poles.

Bode plot of buck converter is shown below:

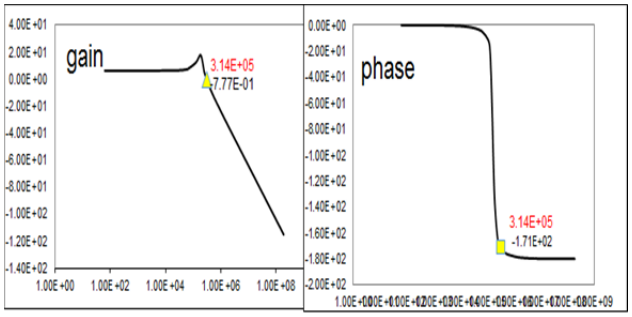

Fig. 4: Transfer function plot of buck converter.

The left side of the plot shows that the double poles are at the peak and right side of the plot shows that the phase margin of the converter is very less indicating a clear possibility of oscillations in the system.

4. PROPOSED BUCK CONVERTER CIRCUIT

This section talks about our proposed circuit and circuit specifications.

4.1. Circuit Specifications

There are many factors that are considered while designing a buck converter like power efficiency, transient response, settling time, output voltage ripples, stability of system and occupied area in the chip. [4]

Table 1 shows the specifications for designing proposed buck converter.

Table 1: Buck converter specifications.

Parameter	Value
Technology	350 nm CMOS process
Input voltage	3.3 V
Output voltage	1.5 V
Maximum output overshoot	10% Vout
Normal maximum load current	500m A
Filter inductor L	3.3u H
DCR of buck	320m Ohm
Filter capacitor C	10u F
R_ESR	20m Ohm

Switching frequency	1M Hz
Line regulation	5% Vout
Load regulation	25m V
Load transient response	150m V
Reference voltage	0.75 V
Ramp amplitude	0.75 V + 400m V
Power efficiency	90%

4.2. Proposed Circuit

Fig. 5 [4] shows the proposed circuit for designing buck converter:

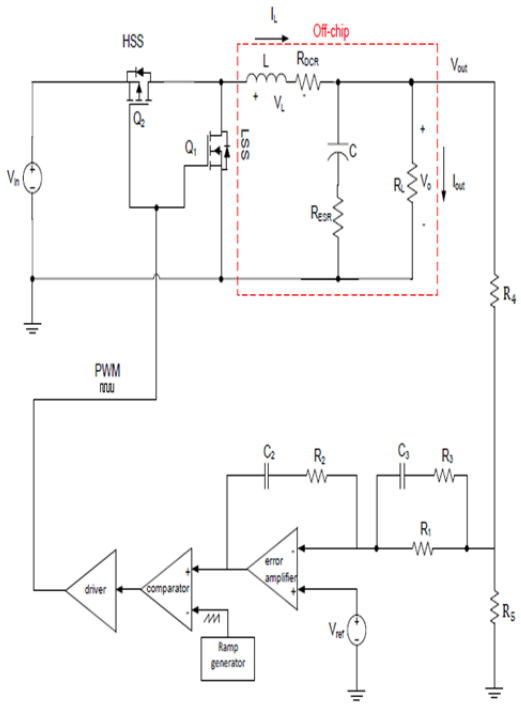

Fig. 5: Circuit diagram of proposed buck converter.

The power stage consists of a dc voltage supply V_{in}, a high side switch Q_2 (PMOS), a low side switch Q_1 (NMOS), inductor L, capacitor C with their resistances in series with them and load resistance R_L. Section 2.1 explains power stage working of buck converter. The replacements of simple switches by Q_1 and Q_2 are for better efficiencies as they have lesser voltage drops across them.

The Buck converter uses a negative feedback control system to regulate the output voltage. As seen in the open loop transfer function of the buck converter (Fig. 4), there exists a double pole which needs to be compensated through this feedback control. The feedback control also serves as a voltage to time converter by providing a PWM control which is proportional to the change in the output voltage. The various blocks involved in the control loop are compensation network, error amplifier, Ramp generator, Duty comparator and Gate drivers.

The error amplifier generates an error voltage which is proportional to the change in the output voltage. This error voltage along with the ramp is used to generate a PWM which controls the ON/OFF time of the HSS and LSS switches. The PWM conversion is governed by the equation:

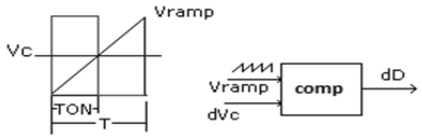

Fig. 6: Vramp vs duty cycle.

From symmetric triangles in Fig. 6, we have

Vramp/T = Vc/TON

TON/T = Vc/Vramp

D = Vc/Vramp ----7

The frequency of the ramp signal is the operating frequency of the Buck converter. For Vc with amplitude at mid-value of Vramp, the duty cycle is 50%. The duty comparator senses the variation in Vc compares it with the ramp signal and produces a varying Duty Cycle.

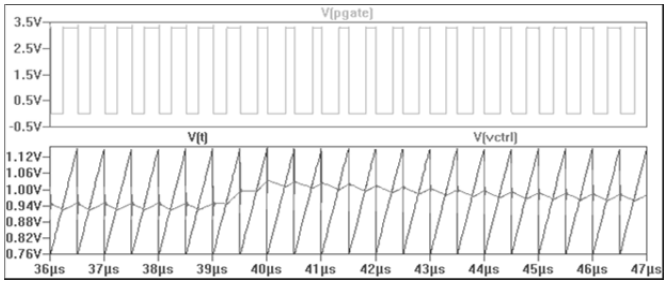

Fig. 7: PWM proportional to change in Vc.

The driver stage in the Buck Converter is very critical. With the power efficiency of the Buck being 90%, the I^2R loss in the switches needs to be minimized. To achieve this , the HSS and LSS switches need to have very small resistance , which due to higher W/L ratio , pose a large capacitance on the gate drivers output. The gate drivers also provide a non-overlapping clock to HSS and LSS which reduces the short circuit power.

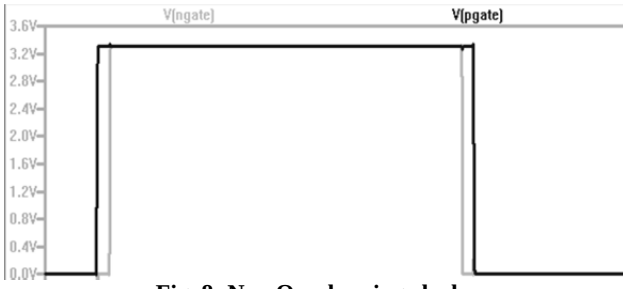

Fig. 8: Non Overlapping clock.

5. SCHEMATIC AND SIMULATION RESULTS

The schematic of proposed circuit and its simulation results are shown below:

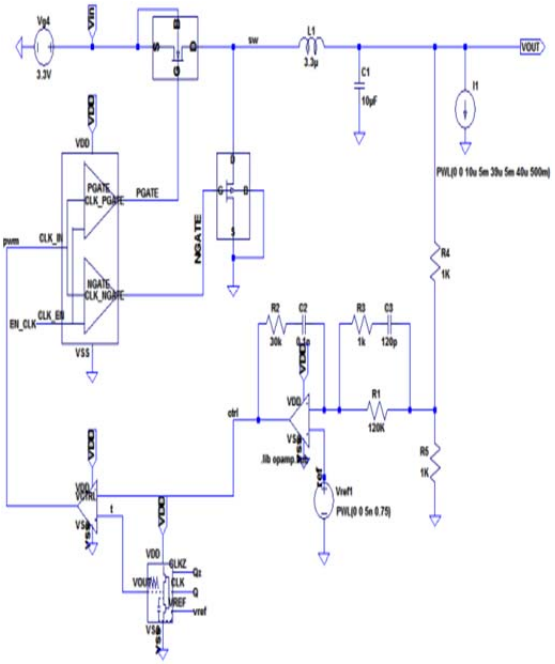

Fig. 9: Schematic of proposed circuit.

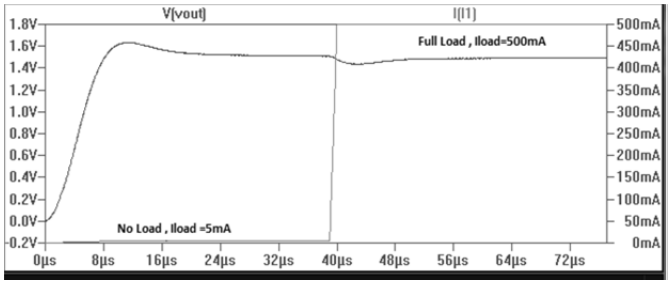

Fig. 10: Output voltage.

As seen in Fig. 10, the output voltage with no Load settles to 1.5V with an overshoot of 130mV. Under full load condition (Iload=500mA), an undershoot of 64mV is observed before the loop recovers.

A load regulation of 10mV (1.5V – 1.49V) is observed when transitioned from no load to full load.

The settling time is measured under no load condition and is observed to be ~20us.

A voltage ripple of 2.3mV is seen at the output regulated voltage as shown in the waveform:

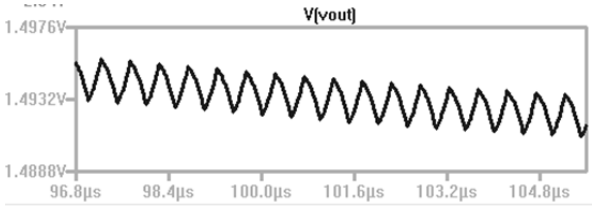

Fig. 11: Output voltage ripple

A line regulation of 25mV is observed for an input voltage range of 3.0V to 3.6V as shown in Fig. 12.

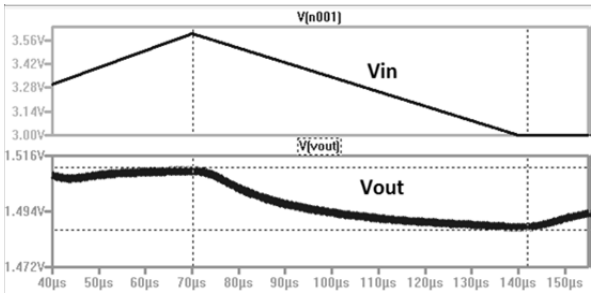

Fig. 12: Line Regulation

6. EFFICIENCY CALCULATION

Buck converter is designed for an efficiency of 90% at maximum lload of 500mA.

Efficiency (η) is given by:

$$\eta = \frac{P_{out}}{P_{in} + P_{loss}} \qquad \text{---8}$$

We know,

- ⇨ $P_{out} = V_o$ * I = 0.75 Watts ---9
- ⇨ $P_{in} = V_{in}$ * I * D = 0.75 Watts ---10
- ⇨ D = V_o/V_{in} = 0.454545455 ---11

Hence, to get an efficiency of 90%, P_{loss} should be ≤ 0.83333333 Watts.

6.1 Budgeting P_{loss}

P_{loss} is defined as a sum of losses at HSS, LSS, L and C.

- ⇨ L loss = (Iload)^2*DCR = 0.008 Watts ---12
- ⇨ C loss = (Iripple)^2*ESR = 0.005 Watts ---13

So, HSS loss = LSS loss = 0.035166667 Watts
But,

- ⇨ HSS loss = (Iload)^2*(D)*RdspON ---14
- ⇨ RdspON < 0.309467 Ohms.

And,

- ⇨ LSS loss= (Iload)^2*(1-D)*RdsnON ---15
- ⇨ RdsnON < 0.257889 Ohms.

Thus, the W/L ratio of HSS and LSS are fixed as to achieve their respective resistances as calculated above to get an efficiency of 90%.

7. CONCLUSION

The buck converter was successfully designed and the parameters were met according to the specifications as shown in the below table:

Table 2: Specifications vs. simulation results.

Parameter	Spec. value	Sim. Results
Technology	350 nm CMOS process	-
Input voltage	3.3 V	-
Output voltage	1.5 V	-
Maximum output overshoot	10% Vout (150mV)	130m V
Normal maximum load current	500m A	-
Filter inductor L	3.3u H	-
DCR of buck	320m Ohm	-
Filter capacitor C	10u F	-
R_ESR	20m Ohm	-
Switching frequency	1M Hz	-
Line regulation	5% Vout (75mV)	25m V
Load regulation	25m V	10m V
Load transient response	150m V	64m V
Reference voltage	0.75 V	-
Ramp amplitude	0.75 V + 400m V	-
Power efficiency	90%	90%

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REFERENCES

[1] en.wikipedia.org/wiki/Buck_converter.

[2] Fundamentals of Power Electronics, Second edition by Robert W. Erickson and Dragan Maksimovic.

[3] Design of converter for low power photovoltaic conversion system by Swapnil Zadey and Subroto Dutt.

[4] Design of a DC/DC buck converter for ultra-low power applications in 65nm CMOS Process by Naeim Safari